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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,038	07/21/2003	Young-Kai Chen	28-19-3-3	6373

7590 07/11/2005

Docket Administrator (Room 3J-219)
Lucent Technologies Inc.
101 Crawfords Corner Road
Holmdel, NJ 07733-3030

EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,038	CHEN ET AL.	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-15 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The structure which goes to make up the device must be clearly and positively specified. The structure must be organized and correlated in such a manner as to present a complete operative device.

Regarding claim 8, the portion "wherein either the dielectric sidewall has a thickness of 500 to 1500 angstroms or part of the extrinsic portion of the base layer is located between the substrate and an extrinsic portion of the top one of the layers" (emphasis added) makes it unclear what Applicants intend as the invention.

Claims 9-15 are rejected as being depended on rejected claim 8.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-11 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 5,506,427 to Imai.

With regards to claim 8, Imai illustrates in figures 1(A)-4, particularly figure 4, (entire document). Imai discloses in figure 1(H) an integrated circuit comprising: a substrate 10 having a top surface;

collector, base and emitter semiconductor layers 14, 30a/36/32 and 38 of a bipolar transistor, the layers forming a vertical sequence in which intrinsic portions of two of the layers (e.g. 14 and 36) are sandwiched between the substrate and a remaining top one of the layers (e.g. 38);

the base layer comprising an extrinsic portion 30a/32 that laterally encircles a vertical portion of the top one of said semiconductor layers 38; and

a dielectric sidewall 34 being interposed between the vertical portion of the top one of the layers and the extrinsic portion of the base layer; and

wherein the dielectric sidewall has a thickness of 50-200 nm or 500 to 2000 angstroms (col. 3, lines 52-53) which overlaps the claimed 500 to 1500 angstroms.

Regarding claim 9, Imai teaches a dielectric sidewall 34 interposed between the vertical portion of the top layer 38 and the base layer 32.

Regarding claim 10, Imai teaches that the extension 32 of the base layer extends farther away from the substrate 10 than an interface between the top layer 38 and the base layer 36 (see fig. 1H showing that base extension 32 is higher than the base-emitter junction).

Regarding claim 11, Imai teaches that one of the two layers that is sandwiched between the substrate 10 and the top layer 38 may include doped region 12 formed in the substrate 10.

Regarding claim 12, Imai teaches a semiconductor extension 40 (note that 40 is made of polysilicon) to the top layer 38 and that part of the extension of the base layer 32 is located between the substrate 10 and the top layer extension 40.

Claims 8 and 12-15 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 4,962,053 to Spratt et al. ("Spratt").

Regarding claims 8 and 12, Spratt illustrates in figures 1-17, particularly figure 12, (entire document) a substrate10 having a top surface;

collector 22, base 54, and emitter 68, 104 semiconductor layers of a bipolar transistor, the semiconductor layers forming a vertical sequence on the substrate in which intrinsic portions of two of the layers are sandwiched between the top surface of the substrate and a remaining top one of the layers,

the base layer comprising an extrinsic portion that laterally encircles a vertical portion of the top one of said semiconductor layers; and

a dielectric sidewall 44, 84 (figs. 9-11) being interposed between the vertical portion of the top one 68 of the layers and the extrinsic portion of the base layer 54: and

wherein part of the extrinsic portion of the base layer 54 is located between the substrate and an extrinsic portion of the top one 68/104 of the layers.

Regarding claim 13, Spratt illustrates in fig. 12 comprising a dielectric layer 44, a portion of the dielectric layer being located on the extrinsic portion of the base layer 54 and the extrinsic portion of the top one 68/104 of the semiconductor layers being located on the dielectric layer.

Regarding claim 14, Spratt illustrates in fig. 12 the extrinsic portion of the base layer 54 extends farther away from the substrate than an interface between the top one 68/104 of the semiconductor layers and the base layer.

Regarding claim 15, Spratt illustrates in fig. 12 one 54 of the two of the semiconductor layers is a doped region of the substrate.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

As the rejection above discloses the dielectric sidewall has a thickness of 50-200 nm or 500 to 2000 angstroms (col. 3, lines 52-53) which overlaps the claimed 500 to 1500 angstroms and Spratt illustrates the extrinsic portion of the base layer 54 is located between the substrate and an extrinsic portion of the top one 68 of the layers.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
July 6, 2005